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PROGRAMMABLE I/O ELEMENT CIRCUIT FOR HIGH SPEED LOGIC DEVICES

This application is a continuation of Application Serial No. 10/017,666 filed on December 14, 2001. which is now a U.S. Patent 6,686,769

Field of Invention

The present invention relates to the field of digital circuitry and programmable logic devices. More particularly, it relates to an input/output element circuit in a logic device where the input/output element circuit is suitable for interfacing with circuits or devices that use high speed input/output standards, such as memory using the double data rate and zero bus turnaround input/output standards.

Background of the Invention

Programmable logic devices (PLDs) are integrated circuit devices containing a number of logic elements that can be selectively programmed to implement a wide variety of logic circuit designs. PLDs are commonly used in digital electronic systems together with other devices such as processors, bus drivers, and memory devices. For example, a field programmable gate array (FPGA) is a PLD that contains an array of logic blocks that represent the individual elements of the logic circuit design being implemented. Each logic block is programmably configured and the blocks are programmably interconnected to implement a user's desired logic functions and circuit design. Similarly, a complex PLD (CPLD) has a limited number of relatively large, user-programmable logic blocks – each of which is similar to a small PLD – that communicate with each other across an interconnect matrix.

In a PLD, input/output (I/O) terminals are used to provide data, control, address and clock signals to and from the configur ed logic blocks in the device. For example, memory controller logic blocks in FPGAs and CPLDs commonly read to and write from memory such as synchronous dynamic random access memory (SDRAM) or static random access memory (SRAM). The memory may be on the same integrated circuit device as the PLD or on a separate device. As used herein, an "I/O terminal" may refer to a terminal that is used as a unidirectional input terminal, exclusively as a unidirectional output terminal, or as a bidirectional terminal that can be configured to act either as an input or an output terminal at any one time. Since the size of a PLD circuit design depends on the number of logic blocks and the number of I/O terminals available, the use